AF/2813

Attorney Docket No. 030681-366

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Kyo-yeol Lee	Group Art Unit: 2813
Application No.: 10/086,892	Examiner: David L. Hogans
Filed: March 4, 2002	Confirmation No.: 1940
For: Method for Fabricating Group III-V Compound Semiconductor Substrate	Appeal No.: _____

BRIEF FOR APPELLANTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the decision of the Examiner dated May 21, 2004, finally rejecting claims 1-7, 15, 26-30, 34 and 35, which are reproduced in Appendix A of this Brief.

A check covering the requisite fee under 37 CFR 41.20(b)(2) accompanies this Brief. The Commissioner is authorized to charge any fees that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800.

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I. Real Party in Interest

The real party in interest with respect to this application is Samsung Corning Co., Ltd., Co. the assignee of record in this application by virtue of the Assignment recorded on March 4, 2002.

II. Related Appeals and Interferences

There are no other prior and pending appeals, interferences or judicial proceedings known to the Appellants, the Appellants' legal representative, or the assignee which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.

III. Status of Claims

Claims 1-40 are currently pending in this application. Claims 1-7, 15, 26-30, 34 and 35 stand finally rejected and are being appealed. Claims 8-14, 16-25, 31-33 and 36-40 are withdrawn, non-elected species claims which should be rejoined upon the indication of allowance of generic claim 1.

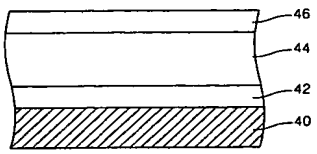
IV. Status of Amendments

No amendments were filed after final rejection. The Examiner's indication on the Advisory Action of October 25, 2004, that an after final amendment would not be entered was apparently made through oversight.

V. Summary of Claimed Subject Matter

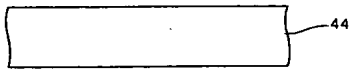
There is only one independent claim on appeal. Claim 1 recites a semiconductor substrate fabrication method having four aspects. First, a base substrate is prepared (see, e.g., page 5, lines 23-26, page 8, lines 32-32, Figure 3, reference 40). This substrate can be, e.g., a sapphire substrate or a silicon carbide (SiC) substrate (see, e.g., page 5, lines 25-26 and original claim 3). Second, a first buffer layer is formed on the prepared base substrate (see, e.g., page 5, lines 23-27, methods 1-3 on pages 6 and 7, experimental examples 1-2, pages 8-10, Figure 3, reference 42). Third, as disclosed, for example, at page 5, line 27 through page 6, line 4 and the methods 1-3 on pages 6-7 and the experimental example 1 and on pages 8-10, a semiconductor layer (e.g., Figure 3, reference 44) is formed on the first buffer layer. This semiconductor layer can be, e.g., a Group III-V compound semiconductor layer having conductivity (page 6, lines 3-4 and original claim 26) such as a silicon-doped GaN layer (page 6, lines 3-4 and original claim 27).

FIG. 3



Fourth, after forming the semiconductor layer, the base substrate is removed such that the semiconductor layer is a final substrate (see, e.g., page 6, lines 7-11, Figure 4, page 9, lines 3-5).

FIG. 4



In various refinements, a second buffer layer (e.g. Figure 3, reference 46) can be formed on the semiconductor layer between forming the semiconductor layer and removing the base substrate (see, e.g., page 6, lines 4-6, methods 1-4 pages 7-8, page 9, lines 1-3, and original claim 2), and the second buffer layer can have the

same structure (e.g., original claim 4) and /or symmetric or asymmetric doping profiles relative to the first buffer layer (e.g., original claims 5 and 6), and even multiple layer embodiments of these first and second layers (e.g., original claims 7 and 15).

Though not part of the claims, embodiments of the present invention solve a problem found in the prior art by minimizing stress occurrence during the growth of the substrate to thereby prevent or reduce the occurrence of cracking.

VI. Grounds of Rejection to be Reviewed

A. Claims 1-7, 15, 26-30, 34 and 35 stand rejected under 35 US.C. § 112, first paragraph, based on the allegation that the specification is non-enabling for the claimed subject matter.

B. Claims 1 and 3 stand rejected under 35 U.S.C. § 102(a) as allegedly being anticipated by Japanese patent publication 2000-105321 to Toshiba (hereinafter "the Toshiba publication").

C. Claims 1 and 3 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,905,275 to Nunoue et al (hereinafter "the Nunoue patent").

D. Claims 2, 4-6, 26, 27 and 34 stand rejected under 35 U.S.C. § 103(a) as allegedly being anticipated by the Nunoue patent in view of U.S. Patent No. 5,290,393 to Nakamura (hereinafter "the Nakamura patent").

E. Claims 7, 15, 28-30 and 35 stand rejected under 35 U.S.C. § 103(a) as allegedly being anticipated by the Nunoue patent in view of the Nakamura patent and in further view of U.S. Patent No. 5,847,409 to Nakayama (hereinafter "the Nakayama patent").

VII. Argument

A. The Specification Fully Enables the Subject Matter of Claims 1-7, 15, 26-30, 34 and 35

The rejection of claims 1-7, 15, 26-30, 34 and 35 under 35 U.S.C. §112, first paragraph, based on the Examiner's unsupported allegation that the specification does not reasonably provide enablement for "any type of substrate," although the Examiner admits it is enabling for sapphire and SiC substrates. The Examiner volunteers that he is uncertain if the base substrate can be made of a material comprised of $C_6H_{12}O_6$, polyvinyl chloride, tantalum pentoxide or $LiAlO_2$, indicated he "is uncertain" if the base substrate can be made by a material and suggests that the recitation of a "base substrate" may comprise "any known material" and therefore does not correspond with Applicant's scope of disclosure to the public. This, it is submitted, is not the proper test.

Similar rejections of these claims occur with respect to the "buffer layer" and the "semiconductor layer." The Examiner is basically alleging that the specific disclosure of several species in the application is not sufficient to support a generic recitation, which the Examiner has interpreted beyond a reasonable breadth.

The Legal Standards

The enablement requirement refers to the requirement of 35 U.S.C. §112, first paragraph, that the specification describe how to make and how to use the invention being claimed. The Supreme Court decision *Mineral Separation v. Hyde*, 242 U.S. 261, 270 (1916) set forth the test for enablement as: "Is the experimentation needed to practice the invention undue or unreasonable?" *In re Wands*, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988) confirms this is still the standard. See also

MPEP 2164.01. In this instance, it is not clear that any experimentation would be required as more fully explained below. As identified in MPEP 2164.01(a) the undue experimentation factors include, but are not limited to:

(a) the breadth of the claims;

(b) the nature of the invention;

(c) the state of the prior art;

(d) the level of one of ordinary skill;

(e) the level of predictability in the art;

(f) the amount of direction provided by the inventor;

(g) the existence of working examples; and

(h) the quality of experimentation used to make and use the invention based on the content of the disclosure.

None of these factors have been addressed by the Examiner. Insofar as the initial burden rests on the Examiner to provide reasons for lack of enablement, and the Examiner has provided no explanation regarding any of these factors, it is respectfully submitted that this rejection must fail, as the record does not establish a *prima facie* case of unpatentability. *In re Wright*, 999 F.2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993).

Additionally, as explained below, two working examples and at least seven additional permutations on the working examples are provided. Further, the semiconductor arts have a high level of predictability and have been in existence for more than 50 years. Adding and removing materials on and as part of substrates are the stock and trade of the semiconductor industry. Applicants do not claim that they have found novel materials or novel processes for any of the steps taken.

Rather, it is the unique combination of method steps which lead to the patentable method recited in the claims.

As noted in MPEP 2164.01(a), a conclusion of lack of enablement means that, based on the evidence regarding each of the above factors of the specification, at the time the application was filed, would not have taught one skilled in the art how to make and/or use the full scope of the claimed invention without undue experimentation. It is not evident that any experimentation need be done to carry out the present invention, let alone undue experimentation.

As articulated in MPEP 2164.02, representative examples support the claim genus insofar as the application makes clear that one of ordinary skill in the art would expect the claimed genus could be used in the manner without undue experimentation. Proof of enablement should only be required for other members of the claimed genus only where adequate reasons are advanced by the Examiner to establish a person skilled in the art would not use the genus as a whole without undue experimentation.[1]

The Error Lies in Interpretation.

It is noted that an error in the rejections seems to be based on the Examiner's interpretation of the claims as including such things as substrates made of glucose ($C_6H_{12}O_6$), for instance. As explained in MPEP 2164.04, before an analysis of enablement, it is necessary for an Examiner to construe the claims.

It is axiomatic that during patent examination the pending claims must be given the broadest *reasonable* interpretation consistent with the specification. *In re*

[1] In this regard, it is noted that the semiconductor arts are generally regarded as predictable and well established arts. The amount of guidance or direction needed to enable the invention is inversely related to the amount of knowledge in the state of the art as well as the predictability in the art. *In re Fisher*, 427 F.2d 833, 839, 166 U.S.P.Q. 18, 24 (CCPA 1970).

Morris, 127 F.3d 1084, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1979); *In re Prater*, 415 F.2d 1393, 162 U.S.P.Q. 541 (CCPA 1969). It is respectfully submitted that to interpret terms such as "base substrate" as reading on glucose ($C_6H_{12}O_6$) is inherently unreasonable and not consistent with the specification. Such an interpretation would not have occurred to one of ordinary skill in the art. The word "substrate" in the semiconductor arts is extremely well known and invokes a subset of materials that could be used therefor. Glucose, for instance, certainly would not be a candidate and it appears by the logic of the rejection that the Examiner is asserting that the "substrate" would read on any material, which would not be the "plain meaning" of the term as recognized in the art. "In construing a claim, claim terms are given their ordinary and accustomed meaning unless examination of the specification, prosecution history, and other claims indicates that the inventor intended otherwise." *Nike Inc. v. Wolverine Worldwide, Inc.*, 43 F.3d 644, 33 USPQ2d 1038 (Fed. Cir. 1994). Once one eliminates the unreasonable hypothetical interpretations, the claims are perfectly clear and fully supported with the enabling disclosure found in the specification as originally filed.

Examiner's Uncertainty

Finally, the Examiner has made several assertions that he is "uncertain" if the base substrate, buffer layer and semiconductor layer could be made of other materials. The Examiner's uncertainty is an inappropriate basis for the rejection. He must, instead, meet the initial burden of establishing a reasonable explanation for questioning the enablement provided for the claimed invention. *In re Wright*, 999 F.2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993) (Examiner must provide a reasonable explanation as to why the scope of protection provided by the claim is

not adequately enabled by the disclosure). Examiners are not generally regarded as people of ordinary skill in the semiconductor art and therefore the Examiner's uncertainty, while not being unexpected or surprising, is not germane to the issue of whether the specification would have been enabling to one skilled in the art. There is no reason to doubt the accuracy of the statements made in the specification and the Examiner has not identified any such reason.

For the convenience of the Board, each of the three terms questioned by the Examiner are identified in the immediately following paragraphs, together with citation to various parts of the specification in support of the assertion that the originally filed specification is fully enabling to one of ordinary skill in the art.

"Base Substrate"

As the Office correctly points out, exemplary embodiments of the base substrate is disclosed as being formed of sapphire or a silicon carbide at, for instance, page 5, lines 25 and 26. This base substrate has the common attributes of being able to be treated so as to form a first buffer layer thereon and to be able to be completely removed. The application of buffer layers and the removal of substrate material are both common expedients within the semiconductor arts for a variety of materials, and it is respectfully submitted that one skilled in the art would know what types of materials were suitable for a base layer.

Further, the disclosure of sapphire/silicon carbide and the number of various working examples clearly demonstrates that the invention has been made. Arriving at substitutes for these materials would be well within the skill set of a skilled artisan. Applicant had possession of and disclosed the necessary common attributes or

features of the elements possessed by members of the genus. Accordingly, Applicants respectfully submit that the disclosure is adequate.

It is further noted that the first Office Action issued without this rejection thus indicating the Office's initial comfort with the scope of the disclosure.

Additionally, the allegation that the recitation "base substrate" could cover "any known material" is not correct. Within the semiconductor arts there is a wide variety but limited number of known materials that can be fairly characterized as a substrate. One skilled in the art would not think that a "base substrate" would include glucose ($C_6H_{12}O_6$), as alleged by the Examiner. Alternative materials for substrates, particularly for common materials such as sapphire and SiC, are well known and their description properly omitted. Information which is well known in the art need not be described in detail in the specification. See, e.g., Hybritech, Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1379-80, 123 USPQ 81, 90 (Fed. Cir. 1986) and MPEP 2163 at page 2100-172.

"Buffer Layers"

The Office acknowledges that the specification is enabling for doped and undoped GaN buffer layers but suggests it does not provide enablement for any type of buffer layer. Actually, the specification is very clear in identifying that the buffer layer is disclosed as being a Group III-V compound semiconductor layer for instance, and may be silicon-doped GaN layers or an undoped GaN layer, or a combination thereof. See methods 1 and 2 at pages 6 and 7, for instance. The other disclosed methods illustrate that the buffer layer can be made of several layers. There are several experimental examples as well which identify that the common attributes are that the buffer layer can be formed on a substrate and, at page 10, it is disclosed that

the buffer layer can be different from the compound semiconductor layer and that another common attribute is that it can be removed together with the base substrate in some embodiments. Further, the buffer layer is designed to provide stress relief between the base substrate and the main substrate. All of these features are known attributes of buffer layers of a variety of types.

Therefore, it would not be difficult for one skilled in the art to come up with buffer layer in combination with selected substrate materials that would be adequate to fulfill these identified characteristics given the considerable guidance offered by the present specification. Accordingly, it is respectfully submitted that the specification is fully adequate insofar as the specification amply demonstrates the necessary common attributes or features of the elements possessed by the members of the genus in view of the species disclosed. The emphasis on the GaN material is simply that of an exemplary embodiment.

"Semiconductor Layer"

Like the buffer layer, the semiconductor layer is disclosed as being a Group III-V compound semiconductor substrate, for instance. It is further disclosed that both compound and noncompound semiconductor substrates and other compound semiconductor substrates not mentioned in the specification can be used. Finally, it is noted that at page 10 the Applicants are explicit in stating that the present invention may be embodied in many different forms and the embodiments described in the specification are merely illustrative and not intended to limit the scope of the invention. Multiple variations on the various embodiments are disclosed including two layer structures, multilayer structures, both alternating doped and

undoped semiconductor material layers, etc. It seems clear that persons skilled in the art would be adequately informed as to how to make and use the invention.

It is respectfully submitted that the Examiner misunderstood the legal requirements for an enabling disclosure and interpreted the claims too broadly, which has lead to his continued rejection of the claims. Accordingly, Appellants respectfully urge the Board to overturn the rejection based on 35 U.S.C. §112, first paragraph, as the Examiner has not established a *prima facie* case of obviousness.

B. The Toshiba Publication Does Not Meet the Recitations of Claims 1 or 3

According to the machine generated translation (Exhibit B-1) of the Toshiba publication, the disclosed optical waveguide element includes a sapphire substrate 10 upon which a buffer layer 11, a clad layer 12 and a quantum well layer 13 are formed. An InP cementing layer 22 is bonded to the quantum well layer 13 so that it can be attached to another substrate 20 via a layer of InGaAsP. Thereafter, the substrate 10 is removed.

This Japanese Patent Publication, however, does not meet each and every recitation of the claims, which is necessary for finding of anticipation under 35 U.S.C. §102(a). Specifically, claim 1 calls for *inter alia* after forming the semiconductor layer, removing the base layer such that the semiconductor layer is the final substrate. The Office identifies the semiconductor layer of claim 1 as being met by the clad layer 12 of this Japanese patent publication. However, a clad layer is not a substrate. In fact, substrate 20 of the resulting product is later attached as illustrated in Figure 1d and is disclosed as being made of InP.

Accordingly, Appellants respectfully request that the Board overturn the Examiner's rejection of claims 1 or 3 over this Japanese Patent Publication, insofar as the Examiner has not established a *prima facie* case of obviousness.

C. The Nunoue et al. Patent Does Not Meet the Recitation of Claims 1 or 3

The *Nunoue et al.* patent discloses a gallium nitrite compound semiconductor light emitting device which includes a sapphire substrate 11 having a trench 11a into which is formed a buffer layer 12 and a compound semiconductor multiple layer 13. Later, a portion of the sapphire substrate 11 is removed to expose the underside of the buffer layer 12 and multiple layer 13, as illustrated in Figures 1b and 1c.

However, the *Nunoue et al.* patent does not disclose, teach or suggest removing the base of substrates such that the semiconductor layer is the final substrate. The *Nunoue et al.* patent depends upon the sapphire substrate 11 continuing to exist for its operation, albeit there being a location which was removed to expose the underside of the multilayer 13 and buffer layer 12. Whether one can fairly describe the multiple layer 13 as a semiconductor layer, the *Nunoue et al.* device does not have a semiconductor layer that is a final substrate as recited in the pending claims.

D. The Nunoue and Nakamura Patents Do Not Teach the Subject Matter of Claims 2, 4-6, 26, 27 and 34

The Office Action, noting that the *Nunoue et al.* patent fails to teach or suggest forming a second buffer layer on the semiconductor layer before removing the base substrate wherein the buffer layer has the same structure as the first buffer layer wherein the semiconductor layer is a silicon-doped GaN layer, the Office applies the *Nakamura* patent. The *Nakamura* patent, with reference to Figure 12 relied upon in the Office Action, discloses a Si-doped buffer layer and an Mg-doped

buffer layer on either side of an Si-doped GaN layer positioned on a sapphire substrate.

Other than the obvious defect in the rejection, i.e., the *Nunoue et al.* patent publication does not teach or suggest removing the substrate and the *Nakamura* patent clearly does not cure this deficiency, Applicants also note that the layers are obviously different, one being Si-doped and the other one being Mg-doped. Therefore, the Examiner's characterization of this reference, particularly Figure 12, is inaccurate. Additionally, the Office suggested that placing the second buffer layer on the silicon-doped GaN semiconductor layer would "improve the crystallinity and carrier concentration/mobility of GaN layers." These features may be apparent in the actual structure of Figure 12, which includes five different layers, namely the sapphire substrate, the Si-doped buffer layer, the Si-doped N-type GaN layer, an Mg-doped buffer layer and a p-type Mg-doped GaN layer, in sequence. There is no indication in the *Nakamura* patent that its different buffer layers would improve crystallinity in a system where the second buffer layer is on a semiconductor layer before removing the base substrate.

Insofar as the buffer layers are doped with different materials, it is also respectfully submitted that the recitations of claims 5 and 6 are not met. Claim 5 recites that the second buffer layer has a doping concentration profile symmetrical with the first buffer layer, whereas claim 6 recites that the second buffer layer has a doping concentration profile asymmetric with the first buffer layer. Because the doping profiles are of different materials, the *Nakamura* patent is inappropriately applied.[2]

[2] At page 7 of the final Office Action, the Examiner invokes *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990) suggesting that patentability is said to be based on a particular chosen method, or other variables recited in the claims. Applicants have not done so and therefore the case law is inapposite.

E. The Nunoue, Nakamura and Nakayama Patents Do Not Teach the Subject Matter of Claims 7, 15, 28-30 and 35

The Office again asserts that *Nunoue et al.* patent incorporates the recitations of claims 1 and 2. Appellants have amply demonstrated that this is not the case. With respect to claims 7, 15 and 28-30, the Office also notes that the *Nunoue et al* patent does not disclose first and/or second buffer layers formed in multiple semiconductor layers. The Office suggested the *Nakayama* patent provides appropriate teachings. The *Nakayama* patent actually discloses a superlattice-structured graded buffer layer which is said to restrain the propagation of lattice defects generated in the buffer layer. Be this as it may, there is no reason to think that defects would be a problem in the *Nunoue et al* patent insofar as a relatively small area of the multi-layer structure is exposed by the removal of the substrate. Even if there were motivation for the combination in the prior art, it would not result in the present invention insofar as the *Nunoue et al* patent does not teach the recitations of claims 1 and 2, for instance, as explained above and the Nakayama patent does not supply these missing teachings, nor is it alleged to by the Examiner.

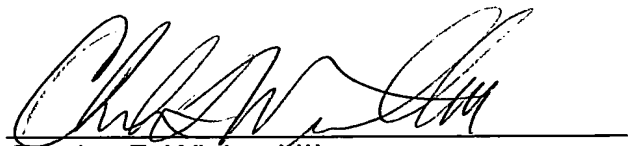
VIII. Conclusion

For the reasons discussed above, Appellants respectfully submit that the Examiner's decision finally rejecting Claims 1-7, 15, 26-30, 34 and 35 should be reversed and such action is earnestly solicited.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: January 21, 2005

By: 

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CLAIMS APPENDIX

The Appealed Claims

1. A semiconductor substrate fabrication method comprising:

preparing a base substrate;

forming a first buffer layer on the prepared base substrate;

forming a semiconductor layer on the first buffer layer; and

after forming the semiconductor layer, removing the base substrate such that said semiconductor layer is a final substrate.

2. The method of claim 1, between forming the semiconductor layer and removing the base substrate, further comprising forming a second buffer layer on the semiconductor layer.

3. The method of claim 1, wherein the base substrate is formed of a sapphire substrate or a silicon carbide (SiC) substrate.

4. The method of claim 2, wherein the second buffer layer has the same structure as the first buffer layer.

5. The method of claim 2, wherein the second buffer layer has a doping concentration profile symmetrical to the first buffer layer.

6. The method of claim 2, wherein the second buffer layer has a doping concentration profile asymmetrical to the first buffer layer.

7. The method of claim 1, wherein the first buffer layer is formed of multiple semiconductor material layers having different doping concentrations.

15. The method of claim 2, wherein the second buffer layer is formed of multiple semiconductor material layers having different doping concentrations.

26. The method of claim 1, wherein the semiconductor layer is a Group III-V compound semiconductor layer having conductivity.

27. The method of claim 26, wherein the Group III-V compound semiconductor layer is a silicon-doped GaN layer.

28. The method of claim 4, wherein the first buffer layer is formed of multiple semiconductor material layers having different doping concentrations.

29. The method of claim 5, wherein the first buffer layer is formed of multiple semiconductor material layers having different doping concentrations.

30. The method of claim 6, wherein the first buffer layer is formed of multiple semiconductor material layers having different doping concentrations.

34. The method of claim 2, wherein the semiconductor layer is a Group III-V compound semiconductor layer having conductivity.

35. The method of claim 15, wherein the semiconductor layer is a Group III-V compound semiconductor layer having conductivity

EVIDENCE APPENDIX

B-1 Machine generated translated version of Japanese Patent Publication 2000-105321 to Toshiba, entered into the record without Examiner objection on September 21, 2004, with the Amendment After Final dated November 22, 2004.[3]

[3] It does not seem that the new rules governing appeals requires this translation to be listed, but Appellants wanted to be sure it was conveniently available to the Board.

RELATED PROCEEDINGS APPENDIX

(None)